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(54) Semiconductor memory device.

(57) A semiconductor memory device comprises a plurality of memory cell arrays and a plurality of word lines and bit lines. The semiconductor memory device has a plurality of row driving circuits for simultaneously activating a plurality of word lines, and a plurality of a column driving circuits for simultaneously and independently activating a plurality of column selective lines to simultaneously select a plurality of bit lines and a data selector for selecting, from the memory cells selected by the word and bit lines, a memory cell selected by different word lines and bit lines. Thus, a plurality of bits are parallel read out or wtitten into the memory cell arrays.

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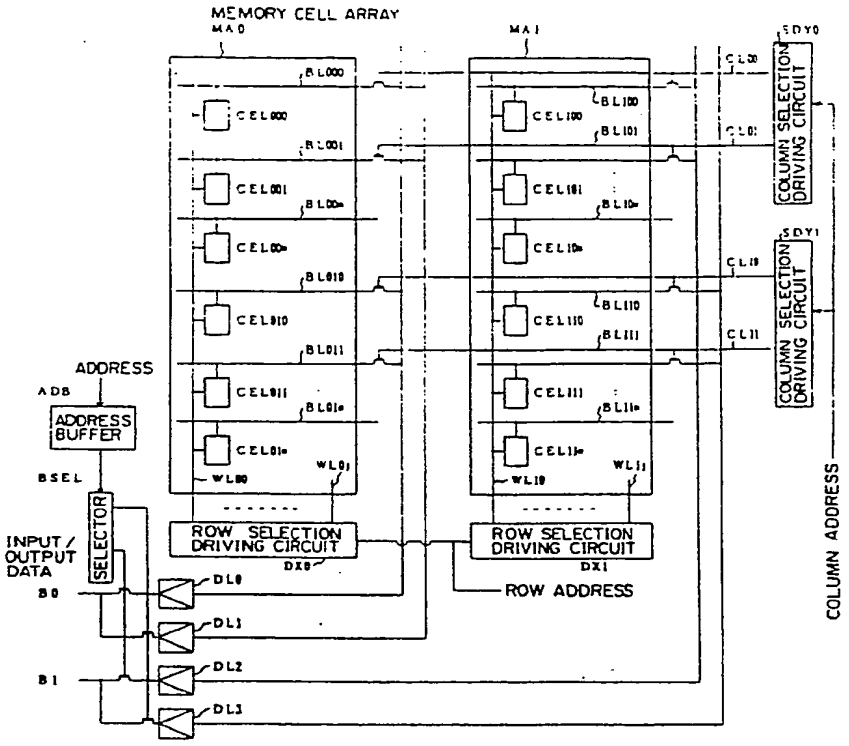


Fig. 3

Semiconductor Memory Device

Background of the Invention

Field of the Invention

The present invention relates to a semiconductor memory device and, more particularly, to a selecting device for selecting memory cells in a dynamic RAM (hereinafter referred to as a DRAM) with a multi-bit input/output configuration.

With recent advances in a fine-structure manufacturing process for large-capacity semiconductor memory devices, it is desired to improve the reliability of the process and the manufactured semiconductor memory devices. To improve the reliability of the semiconductor memory devices themselves, an ECC (Error Correcting Circuit) is used in the system. In general, the Error Correcting Circuit is adapted to detect and correct one-bit error. With the error correcting circuit used in a semiconductor memory devices with multi-bit input/output configurations, if a plurality of bits should fail, errors are not detected and corrected.

Description of the Related Art

Figure 1 illustrates a first example of a semiconductor memory device with a multi-bit input/output configuration.

This memory device includes four memory cell arrays MA0, MA1, MA2, and MA3 and a 8-bit input/output configuration. Each memory cell array, for example, memory cell array MA0, has word lines WL00 to WL0j and bit lines BL00 to BL0m wired in a matrix. A transfer transistor TT and a memory cell (CEL00 to CEL0m) are connected at each word-line/bit-line intersection. Each word line WL00 to WL0j is selected by a row decoder DX0 and driven by a row driver DRX0. An address signal supplied to respective column decoders DY0 and DY1 designates the same address and respective row decoders also designate the same address.

The bit lines are connected to corresponding sense amplifiers SA00, SA01, and so on, in pairs. The sense amplifiers sense and amplify signal variations in the memory cells CEL00 to CEL0m. Output signals of sense amplifier SA00 are read onto a data bus BUS via a transfer gate TG and two bits are latched by data latches DL0 and DL1.

Transfer gates TG0 and TG1 are turned ON or OFF by column driver DRY0 and column decoder DY0 through a column selecting line CL00. This allows bit lines BL00, BL01, BL10 and BL11 to be selected.

Other memory cell arrays MA1, MA2 and MA3 have the same configuration as cell array MA0, described above. Note that column decoder DY0 is shared between memory cell arrays MA0 and MA1 and column decoder DY1 is shared between memory cell arrays MA2 and MA3.

Next, the read operation for stored data will be briefly described.

In reading stored data, two bits are read from an array of sense amplifiers SA for each of the memory cell arrays MA0 to MA3 and data of 8 bits in total are read for application to data latches DL0 to DL7 via data bus BUS. At this point, if a column selecting line CL for any given one of sense amplifiers SA should fail, two bits of 8-bit output data will fail. Detection and correction of two bits cannot be made in the system, making use of the ECC impossible.

Recent advances in wiring techniques and manufacturing processes have given rise to metal-layer interconnected semiconductor memory devices. An example of the metal-layer interconnected semiconductor devices is illustrated in Figure 2. In Figure 2, like reference characters are used to designate parts corresponding to those in Figure 1 and description thereof are omitted.

This semiconductor memory device has eight memory cell arrays arranged in one direction (in the column direction in the Figure) and column select lines CL extended on metal second layers on a substrate board (not shown) to pass across columns of sense amplifiers SA so as to share column select lines CL among the columns of sense amplifiers SA (hence memory cell arrays MA0 to MA7).

Row decoders DX0 to DX7 and row drivers DRX0 to DRX7 are provided for memory cell arrays MA0 to MA7, respectively.

DRs are drivers for driving transfer gates TG which select either of paired memory cell arrays MA0 and MA1; MA2 and MA3; ...; MA6 and MA7 for connection to corresponding sense amplifiers SA.

In this way, because of multilayer interconnection in which column select lines are formed of metal second layers, one column decoder DY for memory cell arrays MA0 to MA7 allows memory cells CEL to be selected and sense amplifiers SA can share column select lines CL, thus permitting high-density integration.

In reading data, one bit is read from each array of sense amplifiers SA and then latched by the corresponding data latch (DL0 to DL3) so that data of 4 bits in total are output through a data bus.

In the above semiconductor memory device, if column select lines CL belonging to any given array of sense amplifiers SA should fail, 4 bits of

output data will all fail. Thus, this semiconductor memory device also cannot use the Error Correcting Circuits, as is the case with the semiconductor memory device of Figure 1.

As in the semiconductor memory devices of Figures 1 and 2, in a semiconductor memory device in which a plurality of bit lines associated with a selected word line through memory cells are activated simultaneously by a common column select line in each memory cell array, if the column select line should fail, many bits will fail simultaneously. Thus, the one-bit-accommodating Error Correcting Circuit cannot be adapted to such a memory device.

Summary of the Invention

It is therefore an object of the present invention to provide a semiconductor memory device of multi-bit input/output configuration in which, if a failure should occur, it will result in a one-bit failure, thus enabling an error correcting circuit to be used in the system.

A feature of the invention resides in a semiconductor memory device comprising a plurality of memory cell arrays each having memory cells connected to a plurality of word lines and bit lines comprises row selective means for simultaneously activating a plurality of word lines; column selective means for simultaneously selecting a plurality of said bit lines by simultaneously and independently activating a plurality of column selective lines and; data selector means for selecting, from memory cells selected said row and column selective means, memory cells which are selected by a combination of different word lines and bit lines.

Brief Description of the Drawings

Figure 1 is a block diagram of a first prior semiconductor memory device; and

Figure 2 is a block diagram of a second semiconductor memory device.

Figure 3 is a diagram for explanaining the principle of the present invention;

Figure 4 is a block diagram of a semiconductor memory device according to a first embodiment of the present invention;

Figures 5A to 5D are diagrams for explanaining the readout of data according to a shifted diagonal system;

Figure 6 is a block diagram of a semiconductor memory device according to a second embodiment of the present invention;

Figure 7 illustrates a circuit arrangement of the data selector of Figure 4;

Figure 8 is a diagram for explanaining addresses for selecting of the data latches of Figure 4;

Figures 9A and 9B are diagrams for explanaining a data latch scan;

Figure 10 is a block diagram of a semiconductor memory device according to a third embodiment of the present invention;

Figure 11 is a block diagram of a semiconductor memory device according to a fourth embodiment of the present invention; and

Figure 12 is a block diagram of a prior column decoder.

Preferred Embodiment of the Present Invention

The embodiment of the present invention will be described by referring to the attached drawings.

A description will be given herein of a two-bit input/output bit configuration.

Figure 3 shows a principle of the present invention.

In Figure 3, a semiconductor memory device has a plurality of memory cell arrays (MA0 to MA1) in each of which memory cells (CEL000 to CEL00m, CEL010 to CEL01M) are placed at intersections of word lines (WL00 to WL0j) and bit lines (BL000 to BL00m, BL010 to BL01M), the present invention is provided with selective drive circuits (SDY0, SDY1) for driving plural bit lines (BL000, BL010) simultaneously among the bit lines (BL000 to BL00m, BL010 to BL01m) associated with a selected word line (WL00) via memory cells (CEL000 to CEL00m, CEL010 to CEL01m).

A case where the input/output bit configuration comprises two bits will be explained herein.

In operation, it is assumed that, in each memory cell array (MA0, MA1, word lines (WL00, WL10) are selected by row-selective drive circuits (DX0, DX1).

In memory cell array (MA0), memory cells (CE000 to CEL00m and CEL010 to CEL01m) are associated with selected word line WL00 and plural bit lines (for example, BL000, BL010) of bit lines (BL000 to BL00m, and BL010 to BL01m) associated with those memory cells are simultaneously selected by column-selective drive circuits (SDY0. SDY1) independently of each other.

Data on simultaneously selected bit lines (BL000 and BL010) are latched by data latches (DL1, DL0) respectively.

In memory cell array (MA1), plural bit lines (BL100 and BL110) of bit lines (BL100 to BL10m and BL110 to BL11m) associated with memory cells (CEL100 to CEL10m, CEL110 to CEL11m) on selected word line (WL10) are simultaneously selected by column-selective drive circuits (SDY0 and SDY1) and independently of each other. Data on

selected bit lines (BL100 and BL110) are latched by data latches DL2 and DL3, respectively.

After being latched by the data latches, one bit is selected from 2 bits read from each memory cell array because the input/output bits are 2 bits, one bit is selected from (DL0, DL1) and one bit is also selected from (DL2, DL3), so that a total of 2 bits (B0, B1) are output. For example, if column selective line CL00 fails, no data will be read into latches DL1 and DL2. However, no data is read simultaneously from latches DL1 and DL2 because of the selecting operation of a selector BSEL, and data will be read from either of latches DL1 and DL2. This will result in a 1-bit error. Thus, even if one word-line/bit-line fails, only one bit fails in input/output data (B0, B1). Therefore, a 1-bit Error Correcting Circuit can be used in an external system.

The 2-bit configuration has been described herein. The same is true of other plural bit configurations.

First Embodiment

Figure 4 illustrates a first embodiment of the present invention which corresponds to the semiconductor memory device of Figure 2. The semiconductor memory device shares column select lines CL among arrays of sense amplifiers SA of memory cell arrays MA0 to MA7 by the use of a second-layer wiring. The first embodiment is the same as the semiconductor memory device of Figure 2 in this respect.

The first embodiment is essentially distinct from the semiconductor memory device in that independent column decoders DY0 to DY3 are used, independent row selective drive circuits DX0 to DX7 are connected to memory cell arrays MA0 to MA7, respectively, row selective drive circuits DX0 to DX7 are selectively switched by block selector BSEL and column decoders DY0 to DY3 and row selective drive circuits DX0 to DX7 are subjected to address control by address signals from address buffer ADB. Address buffer ADB is controlled by timing control circuit TCC which is supplied with a row address strobe signal $\overline{RAS}$, a column address strobe signal $\overline{CAS}$ and a read/write enable signal $\overline{WE}$. As illustrated by MA0, the internal arrangement of memory cell arrays MA0 to MA7 has a memory cell disposed at each word-line/bit-line intersection arrayed in a matrix and it is the same as those of Figures 1 and 2.

Arrays of sense amplifiers SA00 to SA0m, SA10 to SA1m, SA20 to SA2M and SA30 to SA3M have their respective individual row decoders DX0 to DX7 and row drivers DRX0 to DRX7. The number of word lines which are selected simultaneously is equal to or greater than the number of bits in input/output multi-bit configuration (for example, 16 bits in the case of 4-bit input/output configuration). Since the 4-bit configuration is considered herein, four word lines are selected simultaneously. For example, WL00, WL20, WL40 and WL60 are selected simultaneously.

The arrays of sense amplifiers have common column select lines CL0 to CLm. The number of column select lines which are selected simultaneously is equal to or greater than the number of bits in input/output multi-bit configuration. Because of the 4-bit configuration, four column select lines, for example, CL0, CL1, CL2 and CL3, are selected simultaneously.

Therefore, a total of 16 bits of data in 4 rows and 4 columns is latched by data latches DL0 to DL15, each adapted to latch one bit at a time.

A memory-cell selecting device of the present semiconductor memory device is adapted to finally output 4 bits and thus has to take out 4-bit data from 16-bit data. In this case, to permit an Error Correcting Circuit to be used when one word line or column select line fails, data has to be taken out in such a way that, of four output bits, only one bit fails. To this end, 4-bit data has only to be taken out four times by different word lines and different column-select lines. This is performed by data selector DS0 connected to data latches DL2, DL3, DL1 and DL0, data selector DS1 connected to data latches DL6, DL7, DL5 and DL4, data selector DS2 connected to data latches DL10, DL11, DL9 and DL8 and data selector DS3 connected to data latches DL14, DL15, DL13 and DL12. 4 bits are selected from 16 bits by data selectors DS0, DS1, DS2 and DS3 at one cycle and are output from a common data bus.

As such a method of taking out data, from data selector DS0, DS1, DS2 and DS3, there is a shifted diagonal system. Figures 5A to 5D illustrate three examples of data access according to the shifted diagonal system. Figures 5B, 5C and 5D illustrate first, second and third examples of methods of reading data from 16 data latches DL0 to DL15 of Figure 5A, four times four bits at a time. The first and second examples B and C are essentially the same except that they are opposite to each other in the direction of shift. The example of Figure 5D can be said to be a modified shifted diagonal system in that bits are reversed two bits by two bits in the second and third data readout.

For example, in Figure 5A, data in the first row in DL0, DL4, DL8 and DL12 are the contents which will be read simultaneously by activating column selective line CL0. In the event of a failure of column selective line CL0, all bits latched as the first row data will be in error. For this reason, the shifted diagonal systems illustrated in Figures 5B,

5C and 5D allow, when four sets of four bits are read from 16 bits separately, only one bit of failed bits in DL0, DL4, DL8 and DL12 to be read and prevent more than one bit from being read in each cycle of data readout. For example, in the system of Figure 3B, the data of the (1, 1) element is in error, but the data of the (2, 2), (3, 3) and (4, 4) elements are correct in the first period. Thus, only one of the 4-bit data results are in error. In the second period the (2, 1) element is in error and the remaining (2, 3), (3, 4) and (4, 1) elements are correct. In the third period the (1, 3) element is in error and the remaining (2, 4), (3, 1) and (4, 2) elements are correct. Finally, in the fourth period the (1, 4) element is in error and the remaining (2, 1), (3, 2) and (4, 3) elements are correct. In each period, therefore, 4-bit data can be read with one bit in error. The one-bit error can be corrected by an external Error Correcting Circuit. Thus, information will be obtained which is correct in four bits. Therefore, even if the four bits in the first row of 16 bits in figures 5A are all in error, 16-bit information which is correct in all bits will be obtained from the Error Correcting Circuit as long as it operates properly in each cycle. That is, more than three of the 16 bits will be corrected. The same is true of the systems of Figure 5C and 5D.

In summary, as shown in Figure 4, plural bits are output simultaneously by selecting any given word line from memory cell array blocks MA0 and MA1, MA2 and MA3, MA4 and MA5, MA6 and MA7 and any given column select line from common column select lines, and one bit is output from each of respective memory cells so as to fit the number of input/output bits of the data selector of the present semiconductor memory device from the data. Thus, all the bits of output data will not fail and the failure is limited to only one bit even if the word lines or column select lines fail. Therefore, this Error Correcting Circuit can be used, thereby improving the reliability of a semiconductor memory device of a multi-bit input/output configuration.

Second Embodiment

A second embodiment of the present invention is illustrated in Figure 6.

This figure shows an example in which the present invention is applied to a DRAM having 16 memory cell arrays MA0 to MA15. In the Figure, sense amplifiers are excluded from the illustration as they are placed within memory cell arrays MA0 to MA15.

Associated with memory cell arrays MA0 to MA15 are their respective row decoders DX0 to DX15 and row drivers DRX0 to DRX15. 16 memory cell arrays MA0 to MA15 are divided into 4 blocks for 1/4 block operation. In this block operation, a block selector BS is selected by a second pre-decoder PD2 supplied with an address input of two bits A4 and A5 and 1/4 of 16 row drivers are selectively enabled by applying outputs of second pre-decoder PD2 to the row drivers (DRX0 to DRX15). Note that for 1/8 block operation the address input to second pre-decoder PD2 is only required to have three bits.

Associated with the blocks (MA0 to MA3, MA4 to MA7, MA8 to MA11 and MA12 to MA15) are their respective block data latches BDL0, BDL1, BDL2 and BDL3 for each of the 16 bits. Second pre-decoder PD2 enables only one block data latch (for example, BDL0) to allow 16-bit data read from the enabled block to be output to data selector DS4 via block selector BS. In data selector DS4, four bits are selected from 16 bits by first pre-decoder PD1 and outputted.

In the above configuration, a total of four word lines, one for each memory cell array enabled by second pre-decoder PD2, are driven simultaneously and four common column select lines (for example, CL0, CL1, CL2, CL3) are driven simultaneously. Then, data from memory cells at intersections of the different word lines and different column select lines, i.e., data of 16 bits in total, are output from a selected block, latched by a selected data latch circuit (for example, BDL0) and then four bits are finally output from data selector DS4.

Figure 7 illustrates a circuit arrangement of data selector DS4. This circuit arrangement is adapted to the modified shifted diagonal system (refer to Figure 5D. In this Figure are also illustrated exemplary circuit arrangements of data selector DS1 and pre-decoder PD which adapt the "4-bit" input/output configuration to the "1 -bit" configuration by using a method such as a bonding option and AL master slice.

Pre-decoder PD3 receives a 2-bit address input of A0 and A1 and is arranged to provide the "4-bit" input/output configuration when a switching signal S is at a HIGH level and the "1-bit" input/output configuration at a LOW level of switching signal S, thereby converting 4-bit data to 1-bit data. The block data latch circuit (for example BDL0) is comprised of 16 data latch circuits (DL0 to DL15) which are selected by address inputs A0 to A3.

In Figure 7, data selector DS4 selects 4 bits from 16-bit data in block data latches DL0 to DL15 and applies them to common data bus LD4. The shifted diagonal system of Figure 5D is used as the selection system. First, data from DL0 to DL15 belong to block data latch BDL0, not to other blocks, and the data readout of BDL0 is effectively selected by block selector BS. To make this block

selection, only line 4 of pre-decoder PD2 is activated to logic 0 when address inputs A4 and A5 are both at 0 so that pass transistor 15 and all other transistors provided on the right side of transistor 15 are all turned on. The contents of latches DL0 to DL15 are thereby effectively input to data selector DS4. In data selector DS4, 4 bits are selected from 16 bits by activating only one of output lines 8, 7, 6 and 5 of pre-decoder PD1 to logic 1, according to address signals A2, A3 thereto. In pre decoder PD1, line 8 goes to 1 when A2 and A3 are both at 0, line 7 goes to 1 when A2 and A3 are at 1 and 0, respectively. Line 6 goes to 1 when A2 and A3 are at 0 and 1, respectively, and line 5 goes to 1 when A2 and A3 are both at 1. In data selector DS4, 16 pass transistors are placed in the positions illustrated. With this placement, for example, when line 8 is at a logic 1, pass transistors 16, 17, 18 and 19, connected to line 8, become ON state. At this point, 4 bits are read from DL0, DL4, DL10 and DL15 onto common data buses 20, 21, 22 and 23 via the source-to drain paths of enabled pass transistors 16, 17, 18 and 19, respectively. In this case, the read four bits correspond to diagonal components DL0, DL5, DL10 and DL15 in Figure 5A and this corresponds to the first data readout in Figure 5D.

When line 7 is at 1, DL1, D14, DL11 and DL14 are read onto common data buses 20, 21, 22 and 23. These correspond to element (2, 1), element (1, 2), element(4, 3) and element (3, 4) in Figure 5A and this corresponds to the second readout in Figure 5D. When line 6 is at 1, DL2, DL7, DL8 and DL13 are read onto common data buses 20, 21, 22 and 23. These correspond to element (3, 1), element (4, 2), element (1, 3) and element (2, 4) in Figure 5A and this corresponds to the third readout in Figure 5D. When line 5 is at 1, DL3, DL6, DL9 and DL12 are read onto common data buses 20, 21, 22 and 23. These correspond to element 4, 1), element (3, 2), element (2, 3) and element (1, 4) in Figure 5A and this corresponds to the fourth readout in Figure 5D.

That is, the shifted diagonal system is implemented by data selector DS4.

The system for selecting 4 bits from 16 bits has already been described. To select 1 bit from 16 bits, one of the common data buses 20, 21, 22 and 23 is connected to another common data bus LD1 by data selector DS1.

This selection is made by pre-decoder PD3 such that one of row lines 12, 11, 10 and 9 is activated by address signals A0 and A1 when control line S is at 0. More specifically, line 12 is activated when A0 = 0 and A1 = 0, line 11 is activated when A0 = 1 and A1 = 0, line 10 is activated when A0 = 0 and A = 1, and line 9 is activated when A0 = 1 and A1 = 1.

The address signals A0 to A3 described above are internal addresses which are obtained by converting or scrambling external address signals A0 to A3 in accordance with the systems illustrated in Figures 9A and B.

The relation between the selection of the data latches and the logical combination of the address inputs is illustrated in Figure 8. It should be noted here that address inputs A4 and A5 used for dividing the memory cell arrays are not illustrated in Figure 8 because attention is now paid to the selected block (for example, memory cell arrays MA0 to MA3, block data latch BDL0). Figures 9A and 9B show address scrambler circuits and truth tables for implementing them. These tables represent relationships between external addresses and internal addresses. They are implemented when the external address is sequentially incremented with A0 as its least significant bit and A3 as its most significant bit. This causes the data selector to select the data latches in the order of DL0, DL1, DL2, DL3, DL4...DL15 in accordance with a vertical scan shown in Figure 9A. They are also implemented when the external address is sequentially incremented so as to cause the data selector to select the data latches in the order of DL0, DL4, DL8, DL12, DL1, ...DL15 in accordance with a horizontal scan shown in Figure 9B.

The horizontal scan is explained more in detail by referring to Figure 9B. A4 and A5 activate line 4 in Figure 7 when they are (0, 0) and select the output of the data latches DL0 to DL15 by applying the outputs from memory cell arrays MA0, MA1, MA2 and MA3 shown in Figure 6 to block data latch BDL0. When the data latch matrix shown in Figure 8 is scanned in a horizontal direction, data selectors are selected in the order of DL0, DL4, DL8, DL12, DL1, ... DL15. Then, in a case of one bit input and output configuration and in the case where internal addresses A3, A2, A1 and A0 are (0, 1, 1, 0) for example, output line 7 is activated in Figure 7 when A3 and A2 are (0, 1), thereby selecting latches DL1, DL4, DL11 and DL14. Further, when A1 and A0 are (1, 0), a content of data latch DL11 is outputted to common data bus LD1 through output line 10. Namely, when external address 11 is designated by an external pin outside of a chip, the external address becomes a binary code (1, 0, 1, 1) corresponding to the number of 11 and then the internal address becomes (0, 1, 1, 0). thereby enabling a content of DL11 to be read out through the data selector circuit shown in Figure 7 In other words, in case of one the bit output, the address value of the external address coincides with the data latch number. In case of four bit output, and where (A3, A2) are (0, 0), for example, data latches DL0, DL5, DL10 and DL15 are selected regardless of the internal addresses (A0,

A1). The above explanation corresponds to the first cycle in Figure 5D. The internal address is used to select a transistor in the data selector so that the data selector provides the output in accordance with a shifted diagonal method.

Accordingly, in the first reading cycle in Figure 50 it is necessary to provide the internal addresses A3 and A2 as being (0, 0) in order to output four bit data from DL0, DL5, DL10 and DL15 by using the external address. In the truth table of Figure 9B the external address designates one of the addresses (0 00 0), (0 1 0 0), (1 0 1 0) and (1 1 1 1). Therefore, the number of the external addresses in case of the four bit output, decreases to 1/4 that of the external addresses in case of the one bit output.

In a case of the vertical scan, the relation between the input address and the data selector number is the same as that in the horizontal scan and the relation between the external address and the internal address is shown in Figure 9A.

As described above, the method of reading 4-bit data four times by simultaneously driving four word lines and four column select lines in the 4-bit input/output configuration is made possible by use of the circuit of Figure 7. Furthermore, it will also be appreciated that vertical and horizontal scans are made possible by simple scrambler circuits such as that shown in Figure 9 for the 1-bit input/output configuration which is made by the S terminal using bonding option or AL master slice.

Third Embodiment

Figure 10 illustrates a third embodiment of the present invention.

In this embodiment, the present invention is applied to a DRAM in which each row decoder DX0, DX1, ..., DX7 is intervened between its respective memory cell pair MA00 and MA01, MA10 and MA11, MA20 and MA21, ..., MA70 and MA71, each pair being arranged in the row direction, and each row decoder being shared between the paired memory cell arrays. This is a modification of the first embodiment of Figure 4. Like reference characters are used to designate parts corresponding to those in Figure 4 and descriptions thereof are omitted.

In the semiconductor memory device, for example, corresponding word lines WL00 and WL01 in memory cell arrays MA00 and MA01 are selected by the same row address signal (A0) by using one row select driving circuit DX0. Of column select lines corresponding to bit lines BL00 to BL0i connected to memory cells CEL00 to CEL0i which are connected to word line WL00, for example, two column select lines CL0 and CL1, are driven simultaneously so that 2-bit data is output to data latches DL2 and DL3. Also, of column select lines corresponding to bit lines BL0j to BL0m connected to memory cells CEL0j to CEL0m which are connected to word line WL01, for example, two column select lines CL2 and CL3 are driven simultaneously so that 2-bit data is output to data latches DL0 and DL1. Thus, a total of 4 bits of data is output from memory cells MA00 and MA01 to data latches DL0 to DL3.

It should be noted here that the selected word lines WL00 and WL01 have the same address, yet they are not the same address lines and they are mutually independent.

Likewise, 4-bit data connected to different column selct lines is output from each memory cell array block and thus 16-bit data is output to all the data latches. Subsequently, a total of 4 bits is output at a time from each 4-bit block in accordance with the shifted diagonal method shown in Figures 5A to 5D. In this case, even if a failure occurs in a column select line or word line in the memory cell array block corresponding to data latches DL0 to DL3, thus all the data connected to the column select line or word line fail, but only one bit fails of the 4-bit data which is finally output.

Thus, the Error Correcting Circuit is applicable.

Fourth Embodiment

Figure 11 illustrates a fourth embodiment of the present invention.

In this semiconductor memory device, the column select lines are divided into global column select lines (GCL0, GCL1, GCL2,...GCLm) and local column select lines (LCL00, LCL0i, LCL0j, LCL0m, LCL10, LCL1i, LCL1j, LCL1m) and each of the local column select lines is connected to a corresponding global column select line via a switch (SW00, SW0i, SW0j, SWOm, SW10, SW1i, SW1j, SW1m). In the semiconductor memory device, the column selective drive circuit (DY0, DY1, DY2, DY3) is further provided with a spare column decoder (hereinafter referred to as a redundant column decoder, refer to Figure 12) for a failing column select line or column decoder and each memory cell array (MA00 to MA0M, MA10 to MA1m) is provided with a spare memory cell array (hereinafter referred to as a redundant memory cell array, not shown) for failing memory cells. When externally applied address inputs (A0 to Am) are recognized to be defective address inputs, the redundant memory cells are selected by the redundant column decoder. The fourth embodiment is an example in which the present invention is applied to such a DRAM as described above and a modification of the third embodiment of Figure 10. Like reference

characters are used to designate parts corresponding to those in Figure 10.

In this semiconductor memory device, corresponding word lines WL00 and WL01 in memory cell arrays MA00 and MA01 are selected by row selective drive circuit DX0 and data are read from memory cells CEL00 to CEL0m connected to word lines WL00 and WL01 onto their respective bit lines BL00 to BL0m. The operation described so far is the same as that in the third embodiment of Figure 10. However, as an example, four global column select lines GCL0, GCL1, GCL2 and GCL3 may be selected simultaneously from among the column select lines and local column select lines LCL00, LCL0i, LCL0J and LCL0m selected through switches SW00, SW0i, SW0j and SW0m allow data to be latched by data latches DL0, DL1, DL2 and DL3 through BUS. It is this point that is distinct from the third embodiment of Figure 10. The fourth embodiment is the same as the third embodiment in that 4 bits are finally output from 16-bit data read from four blocks one bit at a time from each block by the data selectors in accordance with the shifted diagonal method as shown in Figure 5D. These 4 bits are output by different word lines and different local column select lines, thus permitting the use of the 1-bit Error Correcting Circuit.

The local column select line is made by using a third wiring layer in the multilayer interconnection and is shared among plural memory cell arrays (for example, MA00, MA10, MA20). Of course, the second wiring layer in the multilayer interconnection may be used instead without being shared among memory cell arrays.

Each of the column decoders (DY0 to DY3) of the semiconductor memory device has a redundant column decoder (refer to Figure 12) and each of the memory cell arrays also has redundant memory cells corresponding to the redundant column decoders. The redundant memory cells are excluded from illustration because they are the same in arrangement and number as ordinary memory cells.

Figure 12 illustrates the detail of a column decoder (DY0 by way of example) and means for switching to defective address inputs. In addition to column decoders (CDY0 to CDYm) which operate when normal address inputs for reading normal memory cells a redundant column decoder (CRDY0) is placed. This redundant column decoder operates only when defective address inputs are entered.

A comparison is made between an address signal (10) obtained by amplifying an externally applied address signal (A0 to Am) by address buffer (ADB) and defective address signal (20) output from a defective address storing ROM (ROM) in which defective addresses are stored in advance by a comparator (COM). As a result, when no coincidence occurs, that is, when the externally applied address signal is recognized to be a normal address signal for reading a normal memory cell, one of the global column select lines (GCL0 to GCLm) is selected in accordance with an output (10) of address buffer ADB.

However, as a result of the above comparison, when a coincidence occurs, that is, when the externally applied address signal is recognized to be a defective address signal for reading a defective memory cell, each column decoder (CDY0 to CDYm) is disabled by an output (30) of the comparator (COM) and redundant column decoder (CRDY0) is thereby enabled to select redundant global column select line (GRCL0). That is, when a defective address signal is entered, the redundant decoder is enabled and the corresponding redundant memory cell (not shown) is selected. Therefore, the memory device is viewed from outside as if there were no defect. Although only one redundant decoder is illustrated in Figure 12, it is obvious that plural decoders may be provided.

The switching of column select lines corresponding to defective memory cells to redundant column select lines in order to save the defective memory cells is also effective against row select lines and is thus generally executed. In addition, to improve the efficiency of the redundancy, it is normal to detect defective addresses for each memory cell array (for example, MA00), store them in a defective address storage ROM and determine defective addresses for each of the memory cell arrays.

If a redundancy occures in each of the memory cell arrays in the semiconductor memory device, as switches (SW00 to SW0m, SW10 to SW1m) interposed between the global column select lines and the local column select lines are closed, a problem arises in that the efficiency of the redundancy is lowered, as the column select line is commonly used by a plurality of number cells. For example, suppose that global column select line GCL0 is selected and local column select line LCL0 branched therefrom fails, or is short-circuited in memory cell array MA00. In this case, memory cell arrays MA40 and MA50, whose memory cells are normal, will also be regarded as defective. Thus, where memory cell arrays MA40 and MA50 are selected, switching to redundant column decoder CRDY0 is necessary.

With this semiconductor memory device, therefore, the switches interposed between the global column select lines and the local column select lines are switched by an output (20) of defective address storage ROM (ROM). Even if, for example, global column select line GCL0 is selected and local column select line LCL00 branched therefrom

fails in memory cell array MA00, switch SW00 is opened by the output (20) of defective address storage ROM (ROM), thereby disconnecting the local column select line from the global column select line. When a defective address of memory cell array MA00 corresponding to global column select line GCL0 is selected, switching to the redundant column decoder is performed by such disconnection. However, when memory cell array MA40 is selected, global column select line GCL0 is available as before.

As described above, the column select line is doubled and thus even if two column select lines fail, one bit error output can be obtained according to the present invention, thereby permitting the use of the Error Correcting Circuit.

The above is a description of the case where the column select lines are doubled. If the row select lines area also doubled, the advantage will be further increased. In addition, fuses may be used in place of the switches (SW00 to SW0m, SW10 to SW1m). In this case, a fuse corresponding to a defective address may be blown to disconnect a local column select line from the corresponding global column select line.

According to the present invention, as described above, even if a failure occurs in a word line, a column select line (bit line) or a memory cell in a semiconductor memory device of a multi-bit input/output configuration, not all the bits fail and only one bit definitely results in an error. Therefore, the Error Correcting Circuit becomes available, thereby improving the system's reliability.

Claims

1) A semiconductor memory device comprising a plurality of memory cell arrays each having memory cells connected to a plurality of word lines and bit lines comprises:
row selective means for simultaneously activating a plurality of word lines;
column selective means for simultaneously selecting a plurality of said bit lines by simultaneously and independently activating a plurality of column selective lines and;
data selector means for selecting, from memory cells selected by said row and column selective means, memory cells which are selected by a combination of different word lines and different bit lines.

2) The semiconductor memory device according to claim 1, wherein said row selective means has a plurality of row decoders for receiving a common row address and said column selective means has a plurality of column decodres for receiving a common column address.

3) The semiconductor memory device according to claim 1 wherein,
each of said column selective lines is formed of a first wire layer and said row selective line is formed of a second wire layer.

4) The semiconductor memory device according to claim 1 further comprising a latching means for latching a content of n memory cells selected by said column selecting means, and wherein said data selecting means is connected to the output of said latching means for selecting the content of m of said n memory cells, m being smaller than n.

5) The semiconductor memory apparatus according to claim 1, further comprising an error correcting circuit for correcting an error included in data of a memory cell selected by said data selector.

6) The semiconductor memory apparatus according to claim 4, wherein
m read data are read out at times of n/m in a time divisional manner, thereby enabling n data to be read out.

7) The semiconductor memory apparatus according to claim 4, wherein
said data selector selects the data by performing an on and off control of transistors positioned in a shifted diagonal configuration, by using a signal obtained by decoding a part of an address signal.

8) The semiconductor memory apparatus according to claim 7, wherein
when 4 bits are outputted from 16-bit memory cells of a 4 x 4 partial array forming a part of a memory cell array.

9) The semiconductor memory apparatus according to claim 4, wherein,
an address signal for controlling a selection of said data selector is obtained by converting an external address.

10) The semiconductor memory apparatus according to claim 2, wherein
a row decoder is provided between a pair of memory cells provided in a row direction, thereby commonly using the row decoder.

11) The semiconductor memory apparatus according to claim 4, wherein
said data selector means comprises first data selector for selecting m_1 data from n bit data, m_1 being smaller than n, and a second data selector for selecting m_2 data from m_1 data, m_2 being smaller than

12) The semiconductor memory apparatus according to claim 4, further comprising a block selecting means connected between said data latching means and said data selecting means, for selecting a single data latch block from a plurality of data latch blocks.

13) The semiconductor memory apparatus according to claim 4, wherein

said data selecting means is connected to a plurality of common data buses for simultaneously outputting a plurality of bits and a single bit output data selector for selecting a single common data bus is connected to said common data bus.

14) The semiconductor memory apparatus according to claim 1, further including a redundant column selecting circuit with redundant memory cells.

15) The semiconductor memory apparatus according to claim 14, wherein
an external address is compared with a redundant address stored in a chip and, upon coincidence, a redundant column selective means for selecting a redundant memory cell is activated and a column selecting means for selecting an ordinary memory cell is made non-active.

16) The semiconductor memory apparatus according to claim 15 wherein
an external address is compared with a redundant address stored in a chip and, upon coincidence, a switch of a sub-selective line corresponding to the external address turns off.

17) The semiconductor memory apparatus according to claim 1, which forms a multi-bit input and output bit line configuration and further comprising a column selecting means for independently and simultaneously selecting a column selecting line, the number of which is more than that of the input and output bit line configuration, wherein a plurality of memory cells for simultaneously outputting or inputting data is provided at respective different row selecting lines.

18) The semiconductor memory apparatus according to claim 1, wherein
said row selecting means includes a row selecting circuit for selecting a redundant memory cell.

19) The semiconductor memory apparatus according to claim 18, wherein
an external address is compared with a redundant address stored in a chip and, upon coincidence, a redundant row selecting line for selecting a redundant memory cell is activated and a row selective circuit for selecting a normal memory cell is made non-active.

20) The semiconductor memory apparatus according to claim 18, wherein
an external address is compared with a redundant address stored in a chip and, upon coincidence, a switch for a sub-selective line corresponding to the external address turns off.

21) A semiconductor memory device comprising
a plurality of memory cell arrays each having memory cells connected to a plurality of word lines and bit lines,
column selecting means for activating a main column selecting line from bit lines connected to memory cells on the same selected word line in respective memory cell arrays and for simultaneously and independently activating a plurality of sub-selecting lines connected to said main selecting line through switches, thereby simultaneously selecting a plurality of bit lines.

22) The semiconductor memory apparatus according to claim 21, wherein
said column selecting line comprises a sub-column selecting line connected through a switch.

23) The semiconductor memory apparatus according to claim 22, wherein
an external address is compared with a redundant address and, upon coincidence, a switch for the sub-selecting line corresponding to the external address turns off.

24) A semiconductor memory apparatus comprising:
a plurality of memory cell arrays each having a memory cell connected at an intersection point of a plurality of word lines and bit lines which are wired in a matrix,
column selecting means for activating a main column selecting line from bit lines connected to memory cells on the same selected word line in respective memory cell arrays and for simultaneously and independently activating a plurality of sub-selecting lines connected to said main selecting line through fuses, thereby simultaneously selecting a plurality of bit lines.

25) The semiconductor memory apparatus according to claim 24, wherein
the sub-column selecting line selecting a failed cell is disconnected by cutting off said fuses.

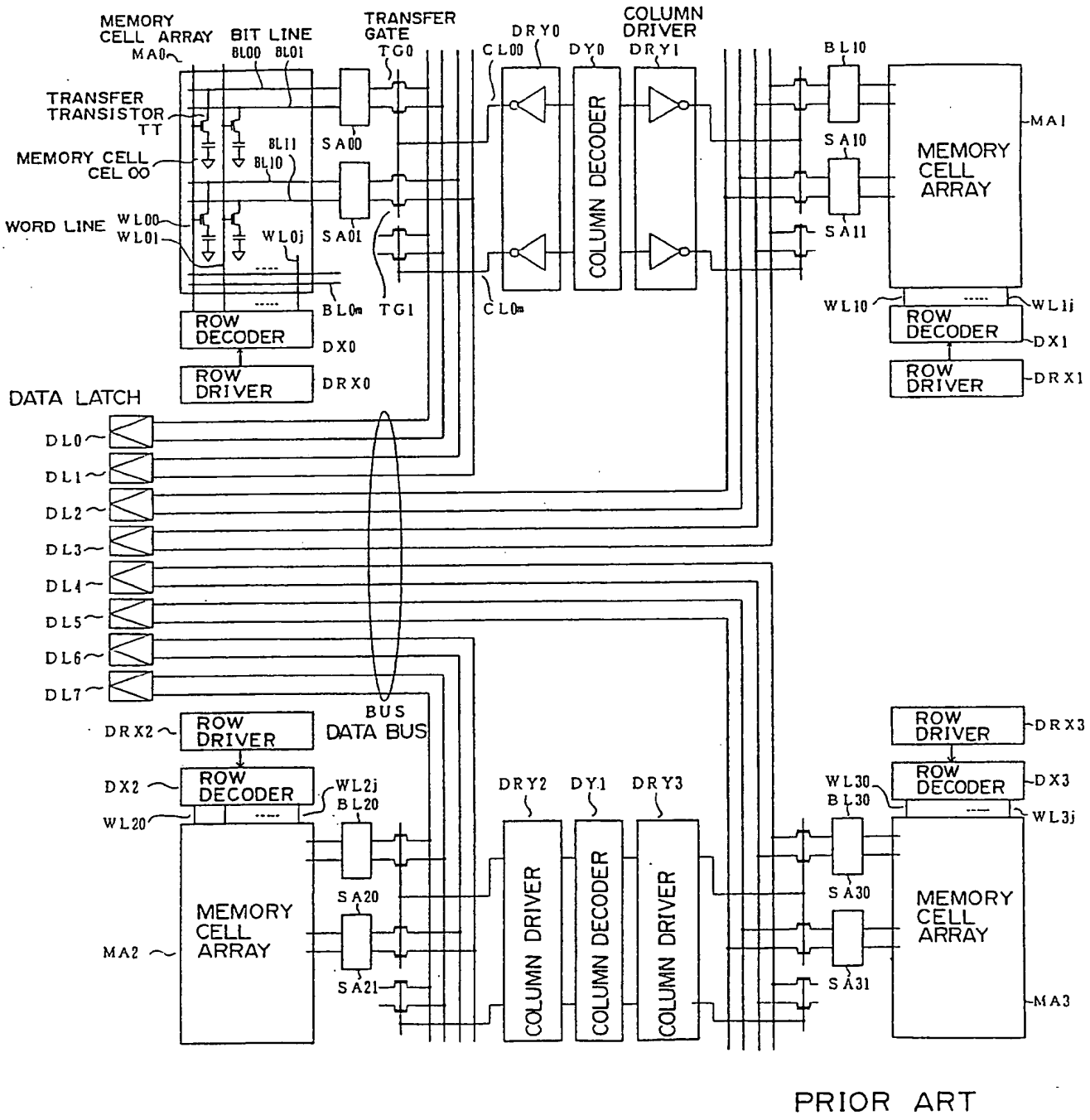
26) A semiconductor memory device comprising:
a plurality of memory cell arrays each having memory cells connected to a plurality of word lines and bit lines which are wired in a matrix, and;
a plurality of means for simultaneously and independently activating a plurality of column selective lines and for simultaneously selecting a plurality of said bit lines selected from among bit lines connected to memory cells by the same word line in said respective memory cell arrays.

27) The semiconductor memory apparatus according to claim 26, wherein
an independently activated column selecting line is connected to a transferring means for transferring the data of the bit line connected to a plurality of memory cells to a bus through a source-drain path

28) A semiconductor memory device having a plurality of memory cells connected to a plurality of word lines and bit lines in an array comprising:
means for simultaneously or independently activating a plurality of column selecting lines when the content of the memory cell connected to said word line is transmitted to the bit line by activating said

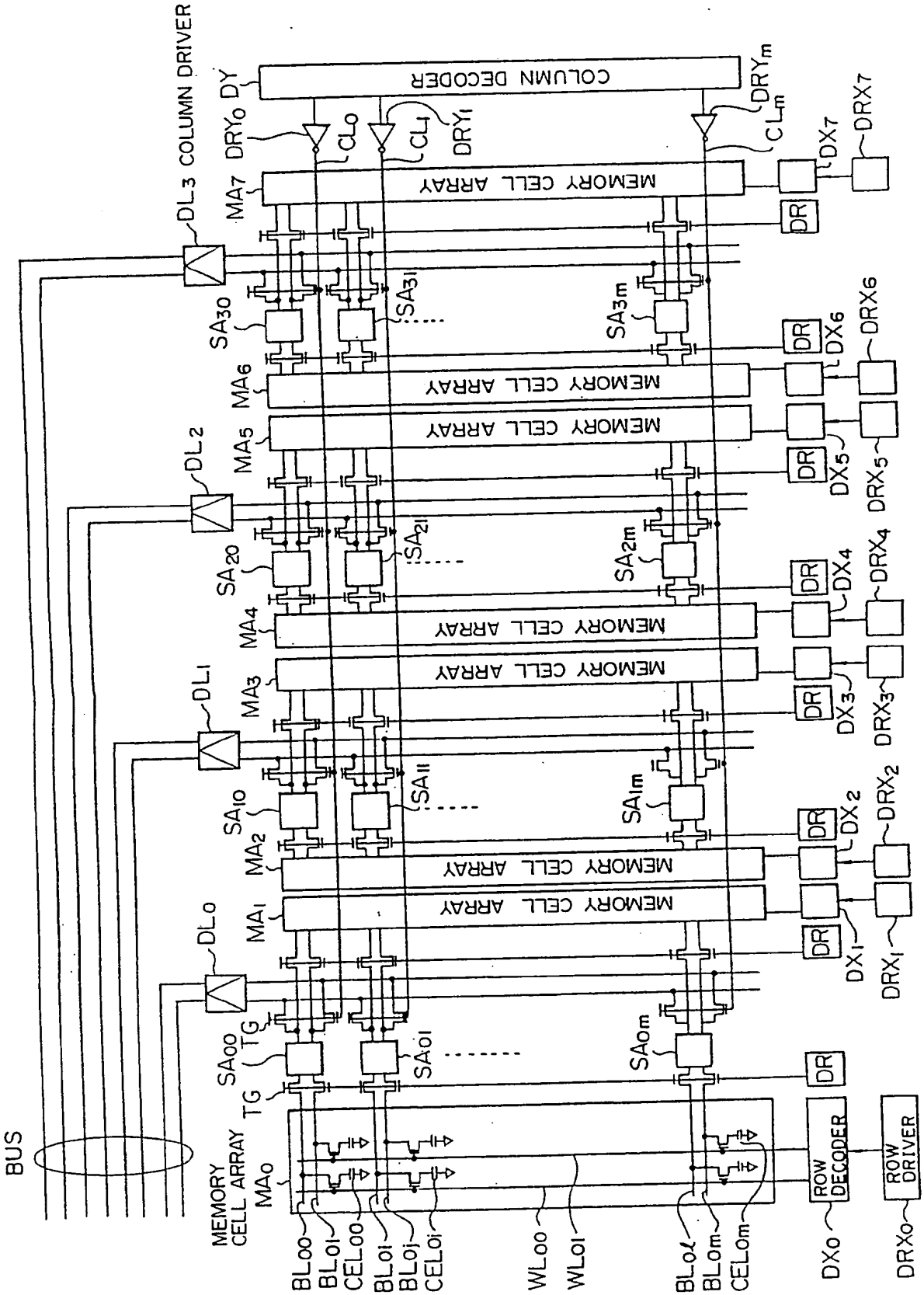
word line and
latching means for latching the content of n memory cells by said column selecting means, and
data selecting means for selecting the contents of m of the n memory cells connected to the output of said latching means, wherein m memory cells are selected by a combination of different word lines and different bit lines.

29) A semiconductor memory device comprising:
means for simultaneously selecting memory cells whose number is larger than the number P of bits to be parallelly input and output and
means for connecting said P memory cells selected by different row lines and column lines to a data bus.



PRIOR ART

Fig. 1



PRIOR ART

Fig. 2

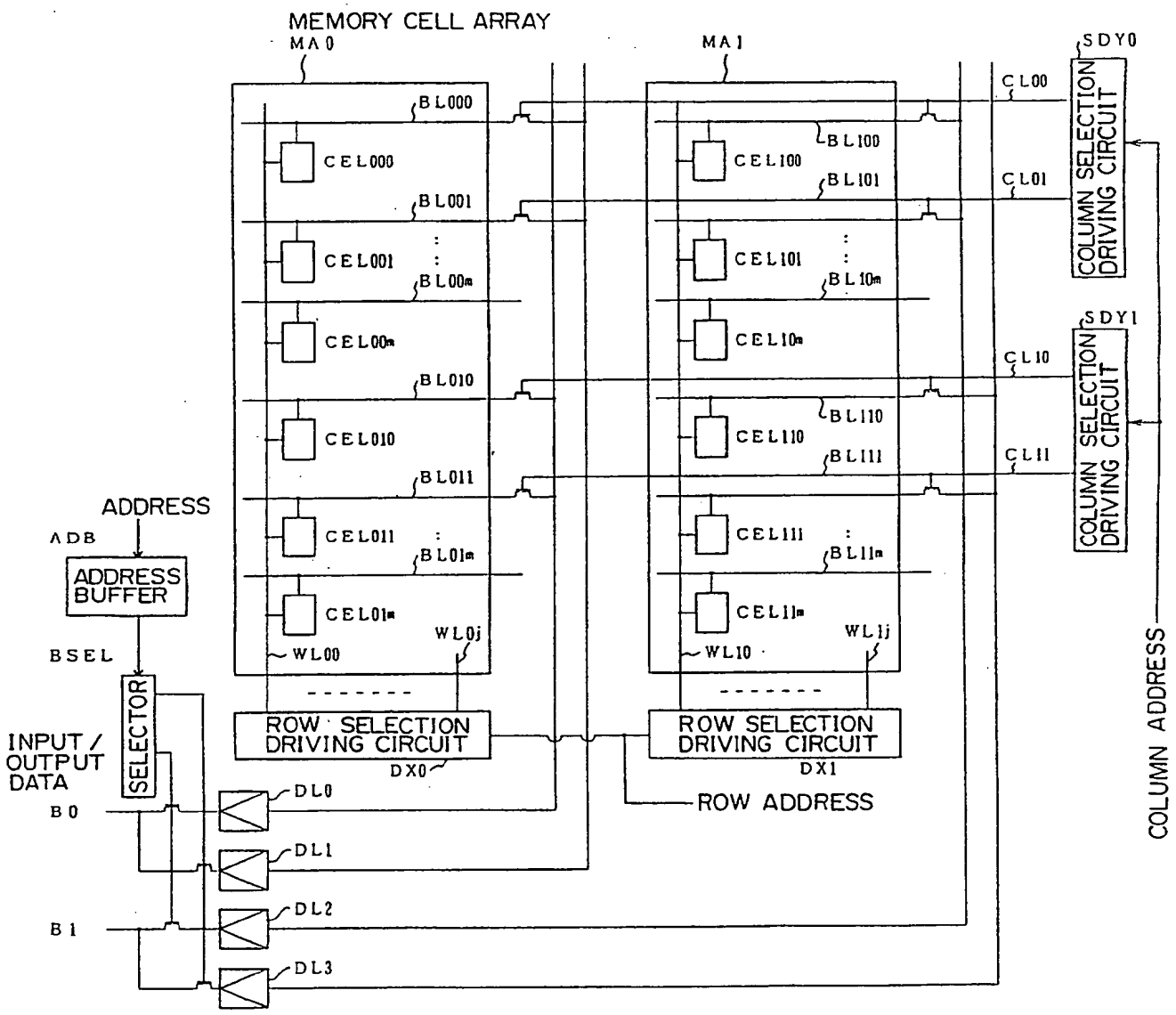


Fig. 3

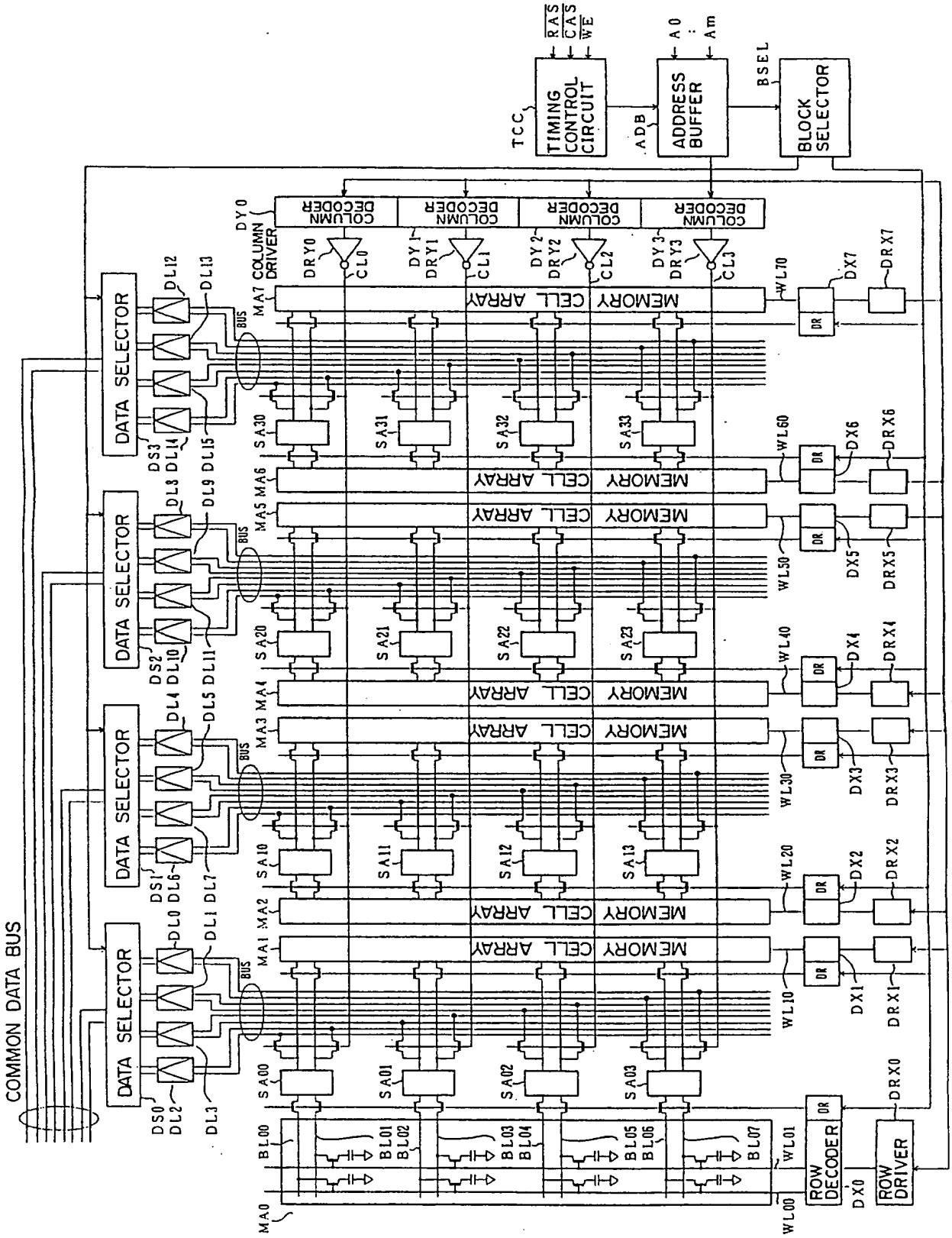


Fig. 4

DATA LATCH				
	DL0	DL4	DL8	DL12
	DL1	DL5	DL9	DL13
	DL2	DL6	DL10	DL14
	DL3	DL7	DL11	DL15

Fig. 5A

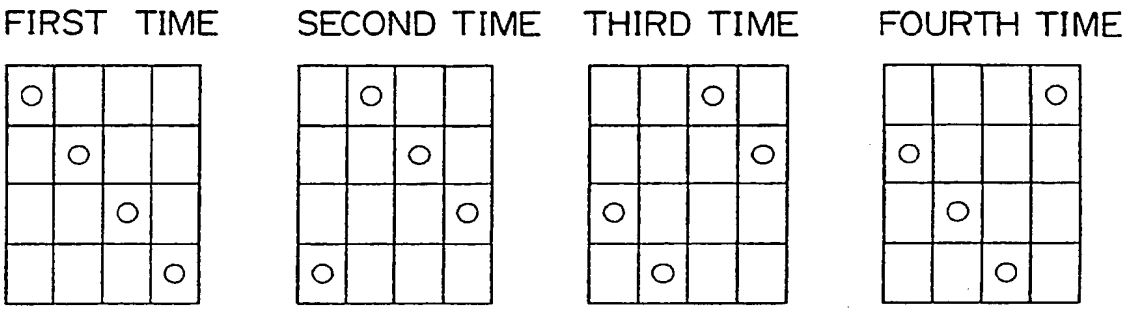


Fig. 5B

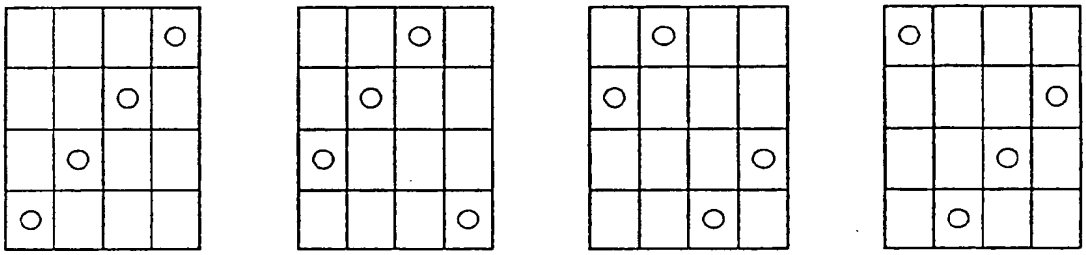


Fig. 5C

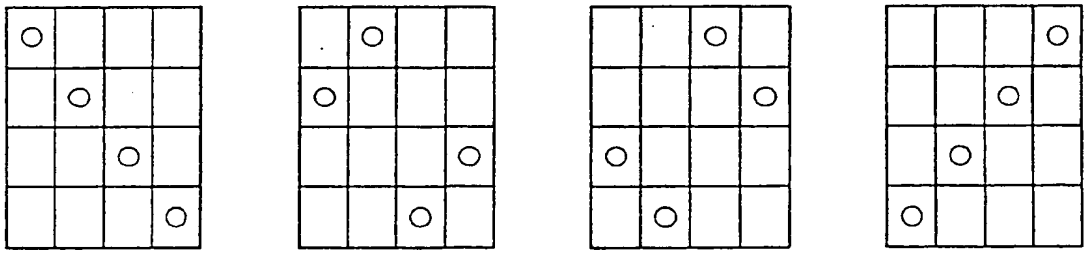


Fig. 5D

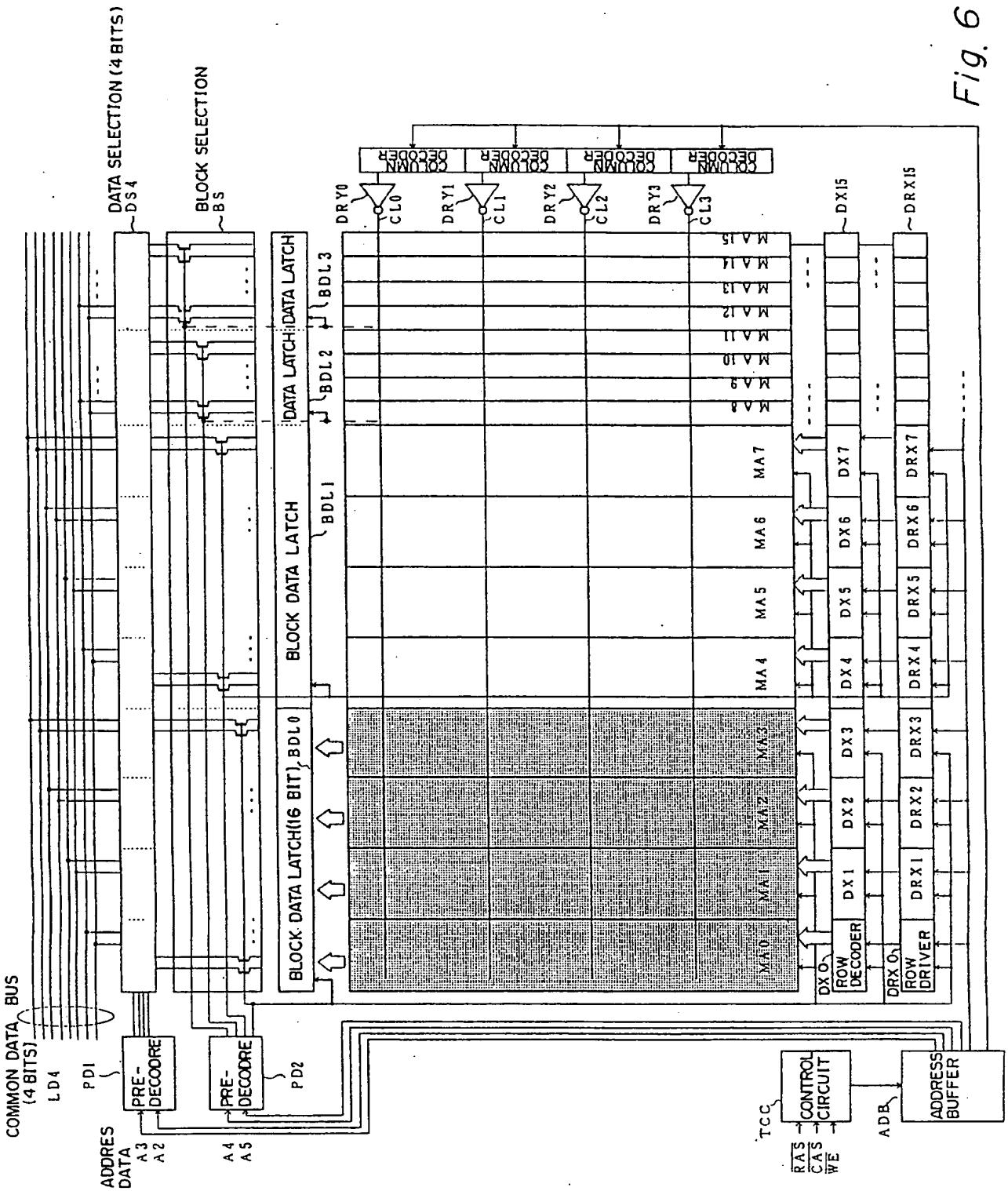


Fig. 6

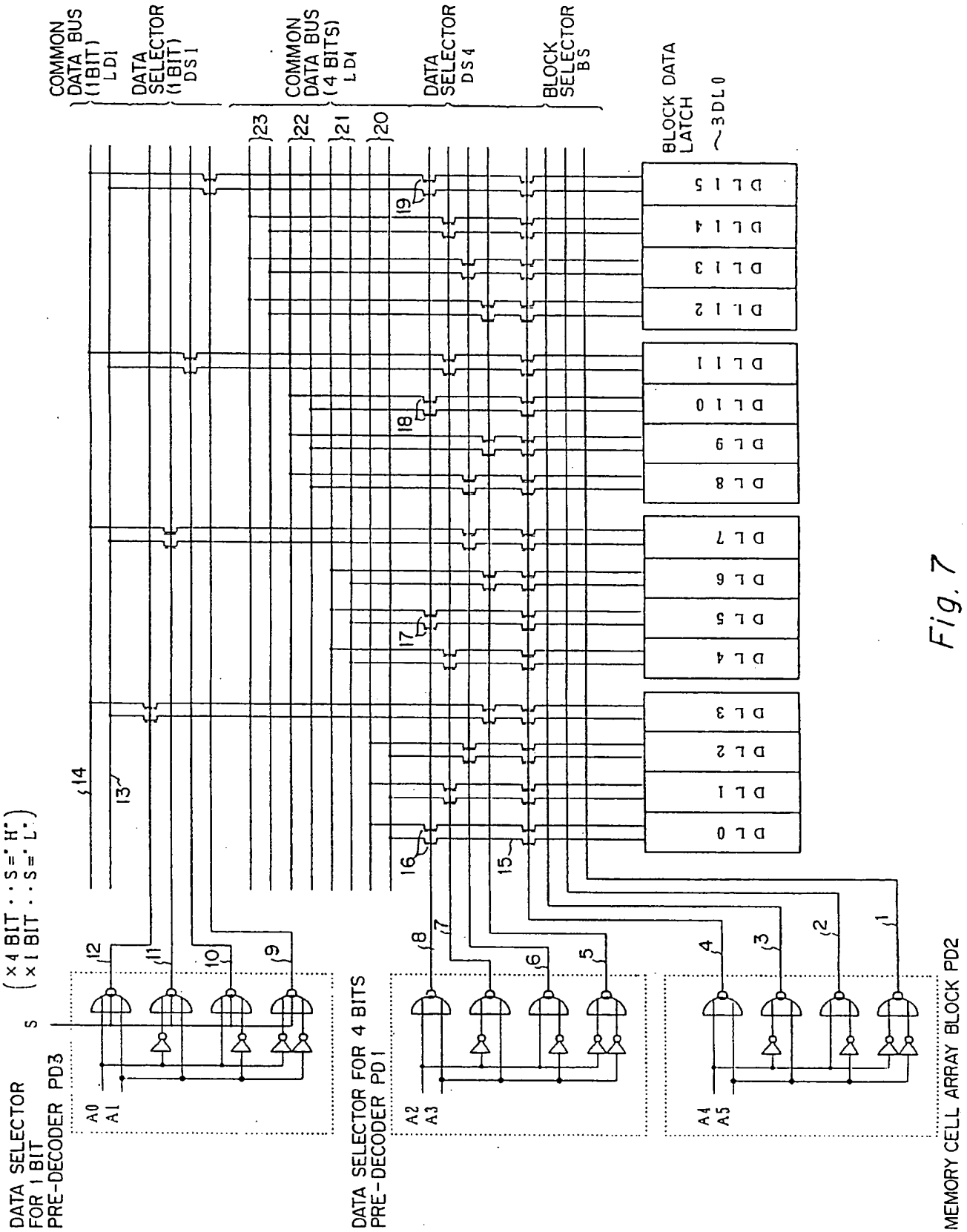


Fig. 7

DATA LATCH

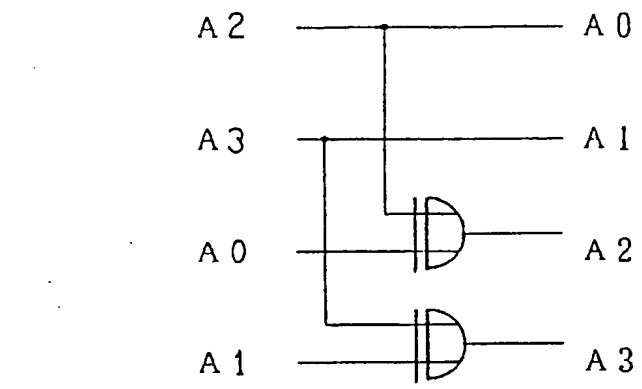
DL 0 A3 A2 A1 A0 0 0 0 0	DL 4 A3 A2 A1 A0 0 1 0 1	DL 8 A3 A2 A1 A0 1 0 1 0	DL 12 A3 A2 A1 A0 1 1 1 1
DL 1 A3 A2 A1 A0 0 1 0 0	DL 5 A3 A2 A1 A0 0 0 0 1	DL 9 A3 A2 A1 A0 1 1 1 0	DL 13 A3 A2 A1 A0 1 0 1 1
DL 2 A3 A2 A1 A0 1 0 0 0	DL 6 A3 A2 A1 A0 1 1 0 1	DL 10 A3 A2 A1 A0 0 0 1 0	DL 14 A3 A2 A1 A0 0 1 1 1
DL 3 A3 A2 A1 A0 1 1 0 0	DL 7 A3 A2 A1 A0 1 0 0 1	DL 11 A3 A2 A1 A0 0 1 1 0	DL 15 A3 A2 A1 A0 0 0 1 1

INTERNAL ADDRESS

(A3, A2 ..... × ON CONSTRUCTING 4 BITS
A3, A2, A1, A0 ..... × ON CONSTRUCTING 1 BIT)

Fig. 8

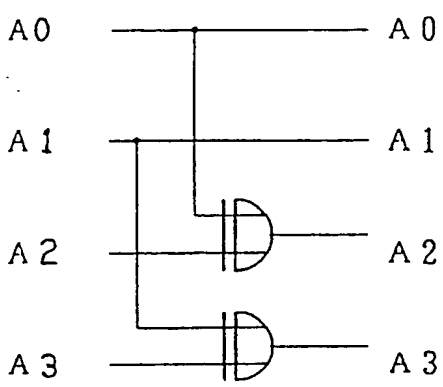
VERTICAL SCANNING OF DATA LATCH



EXTERNAL ADDRESS A3	A2	A1	A0	INTERNAL ADDRESS A3	A2	A1	A0	SELECTION DATA LATCH NO.
0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	1
0	0	1	0	1	0	0	0	2
0	0	1	1	1	1	0	0	3
0	1	0	0	0	1	0	1	4
0	1	0	1	0	0	0	1	5
0	1	1	0	1	1	0	1	6
0	1	1	1	1	0	0	1	7
1	0	0	0	1	0	1	0	8
1	0	0	1	1	1	1	0	9
1	0	1	0	0	0	1	0	10
1	0	1	1	0	1	1	0	11
1	1	0	0	1	1	1	1	12
1	1	0	1	1	0	1	1	13
1	1	1	0	0	1	1	1	14
1	1	1	1	0	0	1	1	15

Fig. 9A

HORIZONTAL SCANNING OF DATA LATCH



EXTERNAL ADDRESS A3	A2	A1	A0	INTERNAL ADDRESS A3	A2	A1	A0	SELECTION DATA LATCH NO.
0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	1	4
0	0	1	0	1	0	1	0	8
0	0	1	1	1	1	1	1	12
0	1	0	0	0	1	0	0	1
0	1	0	1	0	0	0	1	5
0	1	1	0	1	1	1	0	9
0	1	1	1	1	0	1	1	13
1	0	0	0	1	0	0	0	2
1	0	0	1	1	1	0	1	6
1	0	1	0	0	0	1	0	10
1	0	1	1	0	1	1	1	14
1	1	0	0	1	1	0	0	3
1	1	0	1	1	0	0	1	7
1	1	1	0	0	1	1	0	11
1	1	1	1	0	0	1	1	15

Fig. 9B

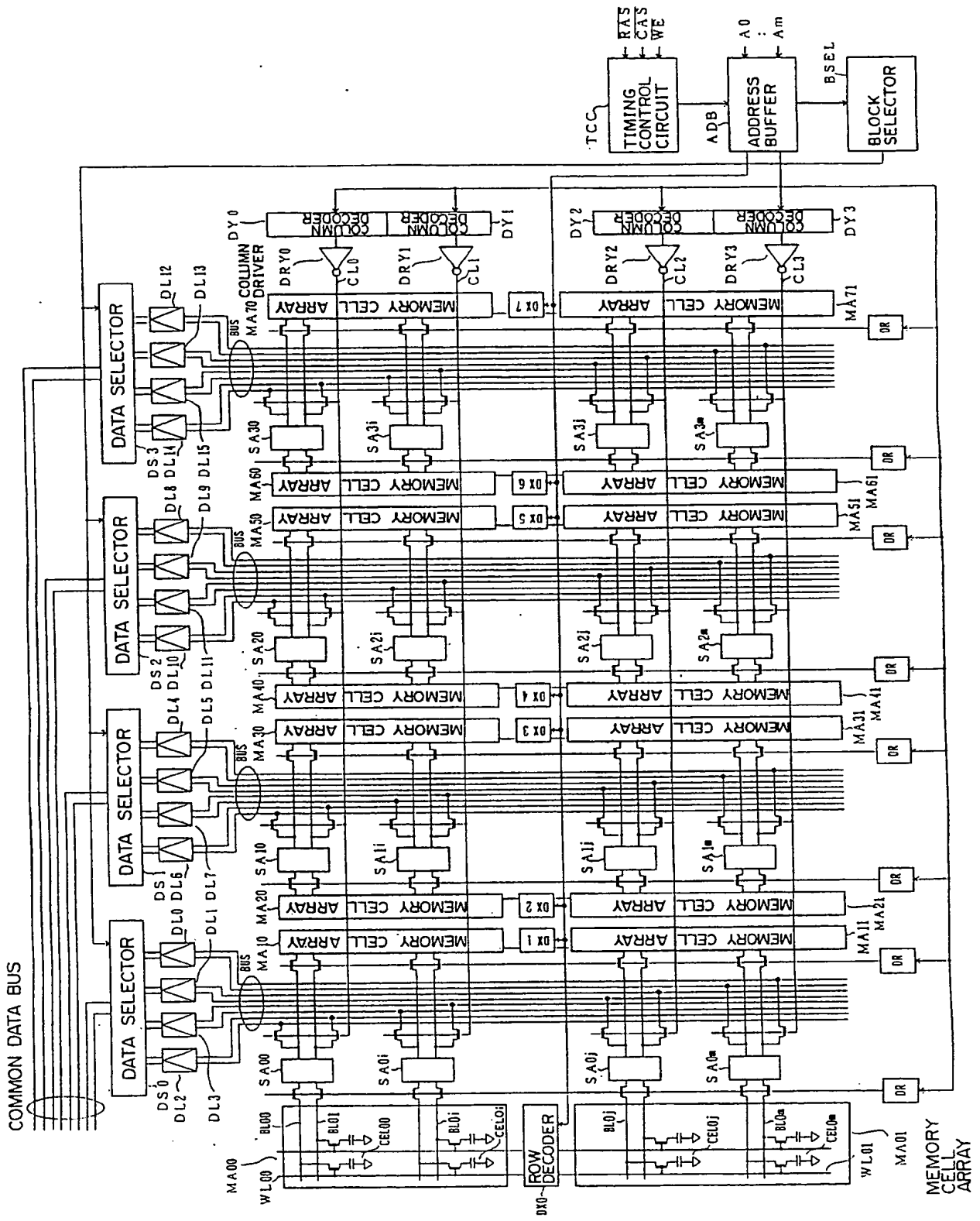


Fig. 10

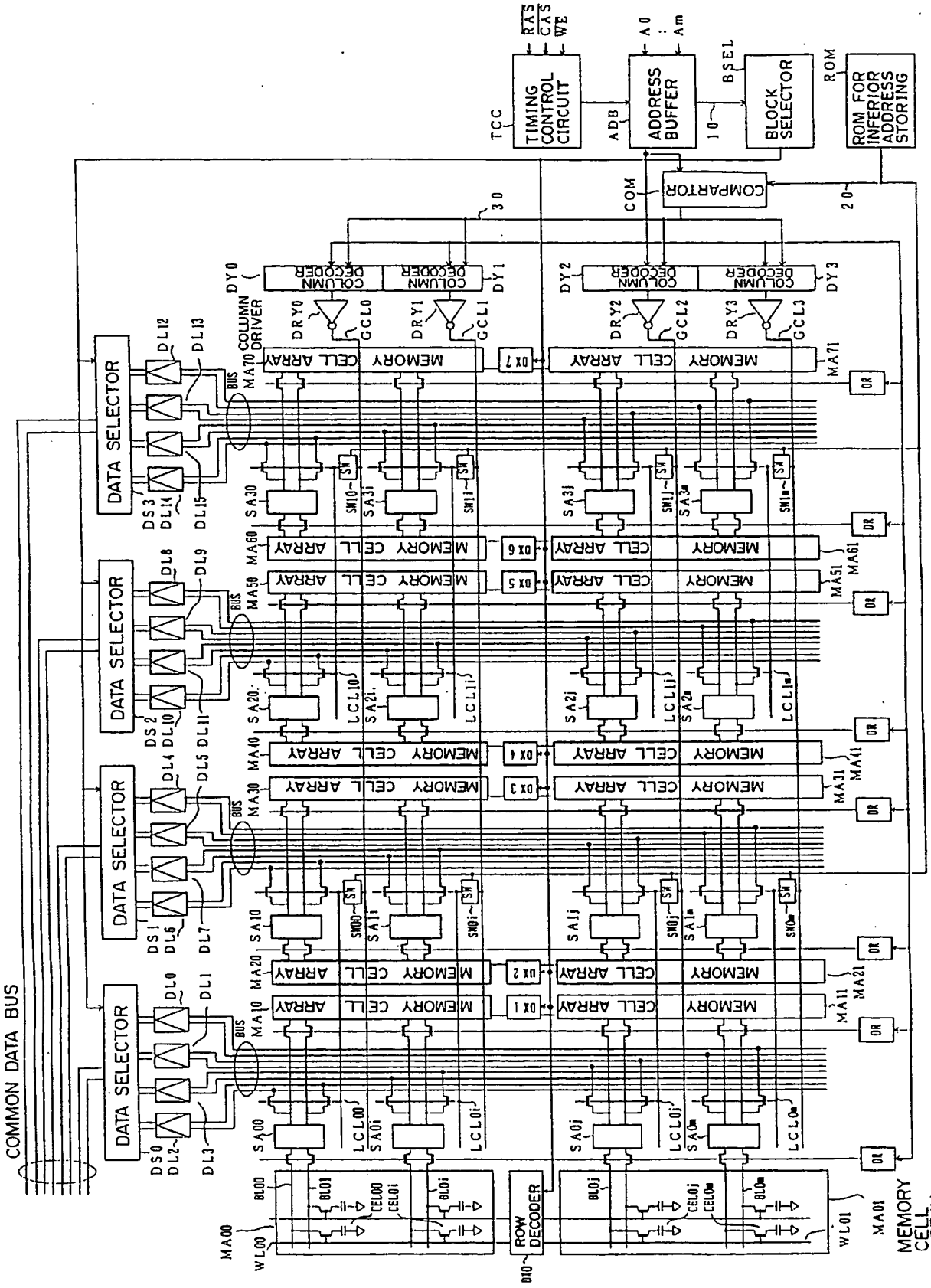


Fig. 11

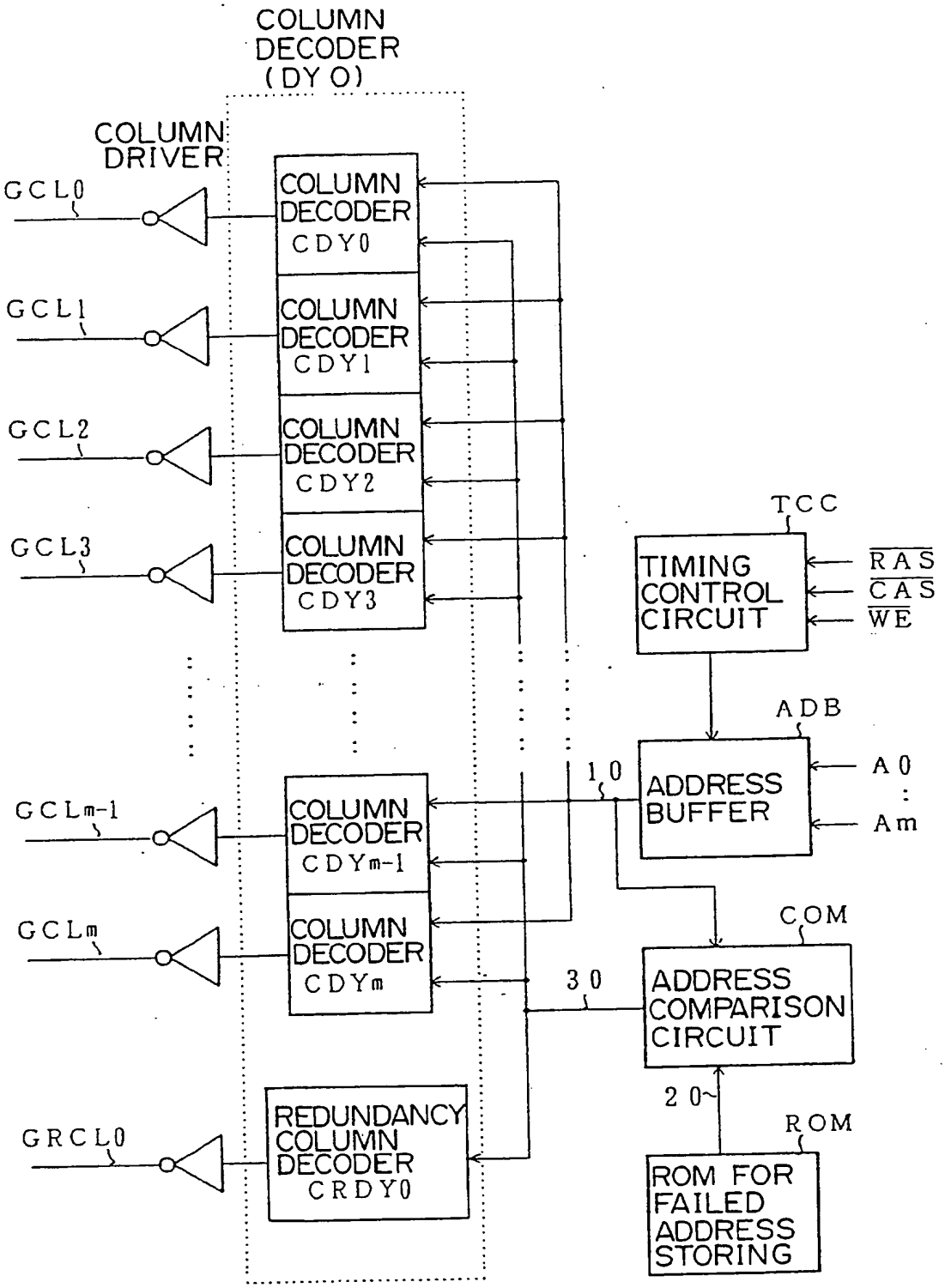


Fig. 12

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European Patent Office
Office européen des brevets

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(54) Semiconductor memory device.

(57) A semiconductor memory device comprises a plurality of memory cell arrays and a plurality of word lines and bit lines. The semiconductor memory device has a plurality of row driving circuits for simultaneously activating a plurality of word lines, and a plurality of a column driving circuits for simultaneously and independently activating a plurality of column selective lines to simultaneously select a plurality of bit lines and a data selector for selecting, from the memory cells selected by the word and bit lines, a memory cell selected by different word lines and bit lines. Thus, a plurality of bits are parallel read out or wtitten into the memory cell arrays.

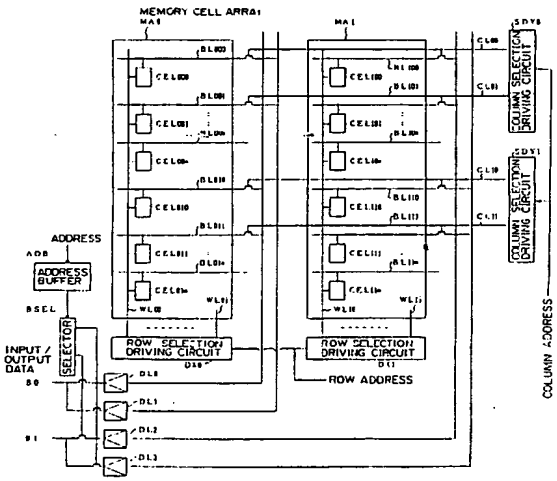

Fig. 3

EP 0 401 792 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 11 0712

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	PATENT ABSTRACTS OF JAPAN vol. 011, no. 236 (P-601)2 March 1987 & JP-A-62 047 900 (TOSHIBA)	1,4,5,9, 13,26,29	G11C7/00 G11C8/00 G11C11/409
A	* abstract *	2,6,11, 17,27,28	G11C11/408
X	IEEE JOURNAL OF SOLID-STATE CIRCUITS. vol. 23, no. 1, February 1988, NEW YORK US pages 20 - 26; YAMADA: 'A 4-MBIT DRAM WITH 16-BIT CONCURRENT ECC'	26,27	
A	* page 22, left column, line 38 - page 23, right column, line 20; figure 6 *	1,2,4,5, 10,13, 21,28	
A	ELECTRONIC DESIGN. vol. 33, no. 4, February 1985, HASBROUCK HEIGHTS, NEW JERSEY pages 121 - 126; BURSKY: 'TECHNOLOGY REPORT: DIGITAL CIRCUITS' * page 128 * * page 130 * * page 132 * * page 134 * * page 136 * * page 136, left column, line 19 - middle column, line 4; figure 5 *	1-3,5, 10,26, 28,29	TECHNICAL FIELDS SEARCHED (Int. Cl.5) G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19 DECEMBER 1991	LINDQUIST J.W.

CATEGORY OF CITED DOCUMENTS

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E : earlier patent document, but published on, or after the filing date
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